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Controller," assigned to the Assignee of the present application, now US Patent
No. 5,944,804, issued 8/31/99

IN THE CLAIMS

Please renumber the claims from 53-69 to 22-38.

Please amend claims 22-38 as follows:

[53]¹~~22~~. (Amended) A method for controlling data transmission over a data network, [the method comprising the steps of]comprising:

copying data to be transmitted from a main memory in a host computer to a buffer memory in a network controller;

transmitting data from the buffer memory over a physical link of the data network in response to a threshold quantity of the data having been copied to the buffer memory from the main memory; and

providing an indication to the host computer that a frame of data has been successfully transmitted from the buffer memory over the physical link of the data network [in response to the frame of data having been copied to the buffer memory]prior to the frame of data being completely transmitted from the buffer memory over the physical link of the data network.

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[54]~~23~~. (Amended) The method of claim [53]~~22~~ [including the additional step of] further comprising unallocating memory locations in the buffer memory upon successful transmission of the frame of data over the physical link.

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[55]~~24~~. (Amended) The method of claim [53]~~22~~ wherein the threshold quantity of data is less than a frame of data.

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[56]~~25~~. (Amended) The method of claim [53]~~22~~ wherein the threshold quantity of data is greater than a frame of data.

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[57]~~26~~. (Amended) The method of claim [53]~~22~~ wherein the network controller monitors transmit events of the data network while transmitting data over the physical link of the data network.

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[58]~~27~~. (Amended) The method of claim [57]~~26~~ wherein the network controller maintains a statistical history of transmit events identified while transmitting data over the physical link of the data network.

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[59]~~28~~. (Amended) An apparatus facilitating the transmission of data over a physical link of a data network, comprising:

a buffer memory having a plurality of memory locations; and

a controller coupled to the buffer memory, the controller to initiate transmission of data from the buffer memory over the physical link in response to

a threshold quantity of data having been copied into the buffer memory from a coupled host computer, the controller to provide to the host computer an indication of successful frame transmission from the buffer memory over the physical link [to the host computer in response to a predetermined quantity of data having been copied to the buffer memory]prior to a complete frame transmission from the buffer memory over the physical link.

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[60]⁸~~29~~. (Amended) The apparatus of claim [59]⁷~~28~~ wherein the [predetermined quantity of data is]the controller provides to the host computer the indication in response to a frame of data having been copied into the buffer memory from the coupled host computer.

[61]⁹~~30~~. (Amended) The apparatus of claim [59]⁷~~28~~ wherein the indication is a transmit complete signal.

[62]¹⁰~~31~~. (Amended) The apparatus of claim [59]⁷~~28~~ wherein the controller monitors transmit events of the data network while data is being transmitted over the physical link of the data network.

[63]¹¹~~32~~. (Amended) The apparatus of claim [59]⁷~~28~~ further comprising a storage medium wherein a statistical history compiled by the controller is maintained.

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[64]33. (Amended) A computer system comprising:

a central processing unit (CPU);

a bus coupled to the CPU;

a main memory coupled to the bus; and

a bus controller coupled between the bus and a physical link of a data network, the bus controller including buffer memory having a plurality of memory locations, the bus controller to initiate transmission of data from the buffer memory over the physical link in response to a threshold quantity of data having been copied into the buffer memory from the main memory, the bus controller to provide to the CPU an indication of successful frame transmission from the buffer memory over the physical link [to the CPU in response to a predetermined quantity of data having been copied to the buffer memory] prior to a complete frame transmission from the buffer memory over the physical link.

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[65]34. (Amended) The computer system of claim [64]33 wherein the

[predetermined quantity of data is] the controller provides to the CPU the indication in response to a frame of data having been copied into the buffer memory from the main memory.

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[66]35. (Amended) The computer system of claim [64]33 wherein the predetermined quantity of data is a frame of data.

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